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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,516	04/16/2004	Husam N. Alshareef	TI 37691	1947

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EXAMINER	
SMOOT, STEPHEN W	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 08/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/826,516	ALSHAREEF ET AL.	
	Examiner	Art Unit	
	Stephen W. Smoot	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6,11,23,25 and 31-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,11,23,25 and 31-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to applicant's amendment filed on 22 May 2006.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Rotondaro et al. (US 2003/0062577 A1).

Referring to Figs. 1A-1E and paragraphs [0014] to [0030], Rotondaro et al. disclose a method of forming CMOS transistors with metal gates that includes the following features:

- A metal layer (40) is deposited over a silicon substrate (20) as shown in Fig. 1A;
- A silicon germanium layer (50) for adjusting the work function of metal layer (40) is deposited over the metal layer (40) as shown in Fig. 1A;
- The silicon germanium layer (50) can be deposited by a plasma enhanced chemical vapor deposition method;
- The silicon-germanium layer is then patterned as shown in Fig. 1B;
- The patterned silicon-germanium layer is then annealed to form a silicon-germanium metal layer (70) with the corresponding adjusted work function as shown in Fig. 1D;
- The silicon-germanium metal layer (70) and the remaining metal layer (40) are then patterned to form gate electrodes 90, 92, respectively, with different work functions as shown in Fig. 1E; and
- An optional cladding layer (100) to reduce sheet resistance that can be tungsten or titanium nitride can be formed over the silicon-germanium metal layer (70) and the remaining metal layer (40) before patterning to form gate electrodes (90, 92) as shown in Fig. 1E and as described in paragraph [0029].

  These are all of the limitations set forth in claims 1-4 of the applicant's invention.

3. Claims 1, 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Woo et al. (US 7,071,086 B2).

Referring to Figs. 3B, 4B and column 3, line 7 to column 5, line 25, Woo et al. disclose a method for tailoring the work function of a metal gate that includes depositing

a metal layer (26) that can be molybdenum, tantalum, or tungsten over a silicon substrate (10) and incorporating silicon into the metal layer (26) by performing a plasma silane treatment (especially see column 4, lines 12-14, 26-54). These are all of the limitations set forth in claims 1, 6 of the applicant's invention.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 6, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilk et al. (US 6,291,282 B1) in view of Woo et al. (US 7,071,086 B2).

Referring to Figs. 3d-3e and column 4, line 4 to column 5, line 49, Wilk et al. disclose a method of forming CMOS devices with metal gates that includes the following features:

- A metal gate electrode (326) that can be tantalum, molybdenum, or titanium is formed over a silicon substrate (301) as shown in Fig. 3d;
- The metal gate electrode (326) is patterned to form gate electrodes corresponding to a PMOS device (302) and to an NMOS device (304) as shown in Fig. 3e;

- The gate electrode corresponding to the NMOS device (304) is masked (328) (i.e. is protected by a mask layer) while the unmasked gate electrode (327) corresponding to the PMOS device (302) undergoes a nitridation treatment to change its work function as shown in Fig. 3e;
- The nitridation treatment preferably occurs by incorporating nitrogen gas in a plasma; and
- An additional layer of conductive material that can be tungsten can subsequently be included with the gate electrodes (326, 327) as described in column 5, lines 44-49.

These are limitations set forth in claims 1-2, 6, 11 of the applicant's invention.

However, Wilk et al. do not expressly teach or suggest the step of subjecting at least a portion of the metal gate electrode material to at least one of a plasma silicidation or plasma germanidation process, which is a limitation of independent claim 1.

Woo et al. teach that the work function of a metal gate layer can be controlled through incorporation of silicon into the metal gate layer using a plasma silane treatment (see column 4, lines 26-54).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Wilk et al. and Woo et al. in order to substitute the plasma silane treatment, as taught by Woo et al., for the plasma nitridation treatment of Wilk et al. Woo et al. recognize that incorporating silicon into a

metal layer is another way to control the work function of a metal gate layer (see column 4, lines 52-54).

6. Claims 23, 25, 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilk et al. (US 6,291,282 B1) in view of Woo et al. and Zhu et al. (US 6,133,079).

Referring to Figs. 3d-3e and column 4, line 4 to column 5, line 49, Wilk et al. disclose a method of forming CMOS devices with metal gates that includes the following features:

- A metal gate electrode (326) that can be tantalum, molybdenum, or titanium is formed over a silicon substrate (301) as shown in Fig. 3d;
- The metal gate electrode (326) is patterned to form gate electrodes corresponding to a PMOS device (302) and to an NMOS device (304) (i.e. field effect transistors) as shown in Fig. 3e;
- The gate electrode corresponding to the NMOS device (304) is masked (328) (i.e. is protected by a mask layer) while the unmasked gate electrode (327) corresponding to the PMOS device (302) undergoes a nitridation treatment to change its work function as shown in Fig. 3e;
- The nitridation treatment preferably occurs by incorporating nitrogen gas in a plasma; and
- An additional layer of conductive material that can be tungsten can subsequently be included with the gate electrodes (326, 327) as described in column 5, lines 44-49.

These are limitations set forth in claims 23, 25, 31 of the applicant's invention.

However, Wilk et al. do not expressly teach or suggest the step of subjecting at least a portion of the metal gate electrode material to at least one of a plasma silicidation or plasma germanidation process, which is a limitation of independent claim 23. Further, Wilk et al. do not expressly teach or suggest forming interconnects within dielectric layers located over the transistors, which are also limitations of independent claim 23.

Woo et al. teach that the work function of a metal gate layer can be controlled through incorporation of silicon into the metal gate layer using a plasma silane treatment (see column 4, lines 26-54). Also, referring to Fig. 4 and column 4, lines 33-61, Zhu et al. teach a method of forming a CMOS structure that includes forming inter level dielectric (ILD) (52) and inter metal dielectric (IMD) (55, 58) layers over field effect transistors (42, 44). The ILD and IMD layers include metal levels (54, 57, 59) that are interconnected using conductive vias (53, 56).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Wilk et al. and Woo et al. in order to substitute the plasma silane treatment, as taught by Woo et al., for the plasma nitridation treatment of Wilk et al. Woo et al. recognize that incorporating silicon into a metal layer is another way to control the work function of a metal gate layer (see column 4, lines 52-54).

It also would have been obvious to a person of ordinary skill in the art at the time the invention was made to further combine the combination of Wilk et al. and Woo et al.

with the teachings of Zhu et al. in order to include the formation of overlying dielectric layers with interconnections, as taught by Zhu et al. Zhu et al. recognize that a multi-level metallization network is used in integrated circuits for wiring discrete semiconductor devices (e.g. field effect transistors) together to thereby create desired circuits (see column 1, lines 14-19).

7. Claims 23, 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rotondaro et al. (US 2003/0062577 A1) in view of Zhu et al. (US 6,133,079).

Referring to Figs. 1A-1E and paragraphs [0014] to [0030], Rotondaro et al. disclose a method of forming CMOS transistors with metal gates that includes the following features:

- A metal layer (40) that can be cobalt is deposited over a silicon substrate (20) as shown in Fig. 1A;
- A silicon germanium layer (50) for adjusting the work function of metal layer (40) is deposited over the metal layer (40) as shown in Fig. 1A;
- The silicon germanium layer (50) can be deposited by a plasma enhanced chemical vapor deposition method;
- The silicon-germanium layer is then patterned as shown in Fig. 1B;
- The patterned silicon-germanium layer is then annealed to form a silicon-germanium metal layer (70) with the corresponding adjusted work function as shown in Fig. 1D;

- The silicon-germanium metal layer (70) and the remaining metal layer (40) are then patterned to form gate electrodes 90, 92, respectively, with different work functions as shown in Fig. 1E; and
- An optional cladding layer (100) to reduce sheet resistance that can be tungsten or titanium nitride can be formed over the silicon-germanium metal layer (70) and the remaining metal layer (40) before patterning to form gate electrodes (90, 92) as shown in Fig. 1E and as described in paragraph [0029].

These are limitations set forth in claims 23, 32-33 of the applicant's invention.

However, Rotondaro et al. do not expressly teach or suggest forming interconnects within dielectric layers located over the transistors, which are limitations of independent claim 23.

Referring to Fig. 4 and column 4, lines 33-61, Zhu et al. teach a method of forming a CMOS structure that includes forming inter level dielectric (ILD) (52) and inter metal dielectric (IMD) (55, 58) layers over field effect transistors (42, 44). The ILD and IMD layers include metal levels (54, 57, 59) that are interconnected using conductive vias (53, 56).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Rotondaro et al. and Zhu et al. in order to include the formation of overlying dielectric layers with interconnections, as taught by Zhu et al. Zhu et al. recognize that a multi-level metallization network is used in integrated circuits for wiring discrete semiconductor devices (e.g. field effect transistors) together to thereby create desired circuits (see column 1, lines 14-19).

Response to Arguments

8. Applicant's arguments regarding the above prior art rejections based on Rotondaro et al., filed on 22 May 2006, have been fully considered but they are not persuasive.

The applicant argues that Rotondaro et al. lack the limitation of a plasma silicidation and/or a plasma germanidation process as set forth in independent claims 1, 23. However, the applicant is reminded that for examination purposes, per MPEP section 2111, claims must be given their broadest reasonable interpretation and, further, per MPEP section 2111.01, the words of a claim must be given their plain meaning unless they are defined in the specification. It is noted that the applicant's originally filed specification does not provide an explicit definition for either "plasma silicidation process" or "plasma germanidation process". Accordingly, the process disclosed by Rotondaro et al. meets this claim limitation because it involves the use of plasma (for deposition of the silicon-germanium layer) to change the work function of a metal layer by forming a silicon-germanium metal layer through a subsequent annealing step that can reasonably be interpreted, per MPEP section 2111, to be a part of the process.

Conclusion

9. Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

sws

Stephen W. Smoot

STEPHEN W. SMOOT
PRIMARY EXAMINER